

Notice of References Cited

Application/Control No.

09/733,612

Applicant(s)/Patent Under
Reexamination
MOLLOY, STEPHEN A.

Examiner

Erick Rekstad

Art Unit

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,192,188	02-2001	Dierke, Gregg	386/95
	C	US-5,949,484	09-1999	Nakaya et al.	348/384.1
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	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Aono et al, "A Video Digital Signal Processor with a Vector-Pipeline Architecture, December 1992, IEEE Journal of Solid-State Circuits Vol.27 No.12, Pages 1886-1894
	V	Toyokura et al, "A Video DSP with a Macroblock-Level-Pipeline and SIMD Type Vector-Pipeline Architecture for MPEG2 CODEC", December 1994, IEEE Journal of Solid-State Circuits Vol.29 No.12, Pages 1474-1481
	W	Toyokura et al, "A Video Digital Signal Processor with a Vector-Pipeline Architecture ", 1992, IEEE Solid-State Circuits Conference, Pages 72-73
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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